

Notice of References Cited	Application/Control No. 09/879,197	Applicant(s)/Patent Under Reexamination KOMODA ET AL.	
	Examiner Fred Ferris	Art Unit 2128	Page 1 of 1

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	B	US-6,473,725 B1	10-2002	Schoellkopf et al.	703/15
	C	US-6,028,995 A	02-2000	Jetton et al.	703/19
	D	US-5,838,947 A	11-1998	Sarin, Harish K.	703/14
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NON-PATENT DOCUMENTS

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	U				
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	W	"Efficient Gate Delay Modeling for Large Interconnect Loads", A.B. Kahng et al, IEEE 0-8186-7286-2/96, IEEE 1996			
	X	"Transistor-Level Estimation of worst-Case Delay in MOS VLSI Circuits", M.R. Dagenais, IEEE Transactions on Computer Aided Design, Vol. II, No. 3, March 1992			

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.